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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,472	01/17/2002	Brian N. Kuo	M-12510 US	7503

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PARSONS HSUE & DE RUNTZ LLP
655 MONTGOMERY STREET
SUITE 1800
SAN FRANCISCO, CA 94111

EXAMINER	
PYO, KEVIN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,472	KUO ET AL.	
	Examiner	Art Unit	
	Kevin Pyo	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. Claims 10 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 10 and 15, claims 10 and 15 recites the phrase in lines 4-5 "photodetectors are ..... spaced at an interval corresponding to ½ said predetermined pitch of the slits". It is unclear what is meant by this phrase in accordance with the drawings. Does it mean that the gap between PD1 and PD3 in Fig.1 is ½ of the pitch of the slit (½P)? Clarification is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4-6, 9 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujiie (5,981,936).

Regarding claim 1, Fujiie shows in Fig.5 the following elements of applicant's claim: a) a first circuit path comprising a first transistor (Q1), a current from said photodetector (PD1) being supplied to the first circuit path; and b) a second circuit path comprising a second transistor (Q2), said two transistors connected to form a current mirror arrangement (CM1), said two transistors

being such that the current mirror arrangement provides a signal that is amplified version of the output of the photodetector (col.6, line 27-51).

Regarding claim 2, Fujiie shows in Fig.5 a photodetector (PD1) is in the first circuit path.

Regarding claim 4, Fujiie shows in Fig.6 the following elements of applicant's claim: a) a first photodiode (PD1); b) a first device (CM1) comprising a first circuit path comprising a first transistor (Q1), a current from said photodetector (PD1) being supplied to the first circuit path; and a second circuit path comprising a second transistor (Q2), said first and second transistors connected to form a current mirror arrangement (CM1), said first and second transistors being such that the current mirror arrangement provides for the first device an output signal that is amplified version of the output of the first photodetector (col.6, line 27-51); c) a second photodetector (PD11); and d) a second device (CM11) comprising a third circuit path comprising a third transistor (Q11), a current from said second photodetector (PD11) being supplied to the third circuit path; and a fourth circuit path comprising a fourth transistor (Q12), said third and fourth transistors connected to form a current mirror arrangement (CM11), said third and fourth transistors being such that the current mirror arrangement provides for the second device an output signal that is amplified version of the output of the second photodetector (col.8, line 26-47).

Regarding claims 5, 6 and 9, the limitations therein are shown in Fig.6.

Regarding claim 11, Fujiie shows in Fig.6 the following elements of applicant's claim: a) a first photodetector (PD1); b) a first circuit path comprising a first transistor (Q1), a current (i1) from the first photodetector being supplied to the first circuit path; c) a second photodetector (PD11) and d) a second circuit path comprising a second transistor (Q11), a current (i11) from

the second photodetector being supplied to the second circuit path, wherein there is no feedback in at least one of the two circuit paths.

Regarding claims 12-14, the limitations therein are shown in Fig.6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiie in view of Tachio et al (5,982,206).

Regarding claims 3, 7 and 8, although Fujiie does not specifically mention the use of MOS transistors to form a current mirror circuit, it is well known in the art as disclosed in Tachio et al to form a current mirror circuit using MOS transistors (Fig.1). It would have been obvious to one of ordinary skill in the art to implement the current mirror circuit of Fujiie using MOS transistors instead of bi-polar transistors, since they are art recognized functional equivalents.

6. Claims 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina et al (4,654,525) in view of Fujiie.

Regarding claims 10 and 15, as far as the claim is understood, Ebina et al differs from the claimed invention in that it does not disclose the recited photodetector circuit. However, it

would have been obvious to one of ordinary skill in the art to utilize the photodetector circuit (Fig.6) of Fujiie in the device of Ebina et al in view of improving signal to noise ratio.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nishizono (6,476,954) is cited for disclosing an optical circuit having a current mirror circuit.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Pyo whose telephone number is (571) 272-2445. The examiner can normally be reached on Mon-Fri (with flexible hour), First Mon. off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin Pyo
Primary Examiner
Art Unit 2878

Pkk
4/27/04